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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/722,306	11/28/2000	Yasunobu Iwata	Q61090	5612

7590 03/09/2004

SUGHRUE, MION, ZINN, MACPEAK & SEAS
2100 Pennsylvania Avenue, N.W.
Washington, DC 20037

EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 03/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/722,306	IWATA ET AL.	
	Examiner	Art Unit	
	Helen B Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the application 09/722,306 filed 11/28/2000 and amendment filed 12/03/2003.

2. Claims 1-4 remain pending in the application. Amendment has been fully considered by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Komiya et al. (US Patent 5,126,956).

As to claim 1 Komiya et al. teaches an unavailable area for storing a plurality of previously stored circuit patterns of circuit elements within the character generator (CG) for storing various alphanumeric characters an symbolic patterns illustrative of a ladder diagram as shown on the Fig. 8 including the refresh memory (RFM) which is used for storing a picture information regarding the sequence program (col. 7, ll.28-30; col. 8, ll.63-67); an available area for storing circuit elements of a circuit pattern being input by using a picture memory (IMM) shown on the Fig. 8 for successively storing items of picture data generated by the character generator (CG) (input circuit pattern) based on the picture information given by RFM (col. 7, ll.30-33); circuit pattern extracting means for making a comparison between a circuit element of the circuit pattern being input and

a corresponding circuit element contained in one of the plurality of previously stored circuit patterns stored in the unavailable area, and extracting from the plurality of previously stored circuit patterns an extracted circuit pattern in which the comparison indicates an agreement between the compared circuit elements within the display controller (DPC) shown on the Fig. 8 and depicted in details on the Fig. 11, wherein the process of comparison a circuit element of the circuit pattern as input with one from the plurality of previously stored circuit patterns in the unavailable area (CG) is performed, wherein comparator (COM), controller (CNT), buffer register (BFR) and register (RG) make a conclusion if there is an agreement or non-agreement between those two circuit elements has been achieved (col. 9, ll.20-35); display means for displaying the extracted circuit pattern on an input screen as shown on the Fig. 10 wherein an explanatory view showing as example of a display presented on the screen of a CRT included in the system of FIG. 8 and using a drive (DDV) which receives the picture information as output of the picture memory (IMM) for displaying on the CRT (col. 7, ll.33-38; ll.44-47); and copying means for copying the extracted circuit pattern into the available area in response to an input by an operator within display controller (DPC) shown in details on the Fig. 11 which is operated as copying of transferring data into the available area (IMM) ready for display (col. 9, ll.15-20).

As to claims 2 and 3 Komiya et al. teaches when more than one extracted circuit pattern is extracted, the display means successively displays, for selection by an operator, the plurality of extracted circuit patterns, using display controller (DPC) the operator may select the segment for displaying and as shown on the Fig. 10 wherein an

explanatory view showing as example of a display presented on the screen of a CRT included in the system of FIG. 8 and using a drive (DDV) which receives the picture information as output of the picture memory (IMM) for displaying on the CRT (col. 7, ll.33-38; ll.44-47; col. 8, ll.13-21); in response to the selection of one of the plurality of extracted circuit patterns, the copying means copies circuit pattern into the available (IMM) area within display controller (DPC) shown in details on the Fig. 11 which is operated as copying of transferring data into the available area (IMM) ready for display (col. 9, ll.15-20); the display means displays a previously selected circuit pattern as a top priority within the display controller which stores all selected patterns in the refresh memory (RFM) and after comparison stores them (if it was successive i.e. agreement was reached between a circuit element of the circuit pattern as input with one from the plurality of previously stored circuit patterns in the unavailable area (CG)) in the picture memory (IMM) and then they are displayed sequentially according the conception of the ladder circuit in the sequence program (col. 8, ll.9-12).

Allowable Subject Matter

5. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach a selected circuit pattern address storage area storing an address of a previously selected circuit pattern; and a replacing means for placing the address of previously selected circuit pattern the head of the selected circuit pattern address storage area, wherein the display means displays as a top priority the previously selected circuit pattern according

to an order of addresses stored in the selected circuit pattern address storage area as claimed.

Remarks

6. As to claim 1 Komiya et al. teaches an unavailable area for storing a plurality of previously stored circuit patterns of circuit elements within the character generator (CG) for storing various alphanumeric characters an symbolic patterns illustrative of a ladder diagram as shown on the Fig. 8 including the refresh memory (RFM) which is used for storing a picture information regarding the sequence program (col. 7, ll.28-30; col. 8, ll.63-67); an available area for storing circuit elements of a circuit pattern being input by using a picture memory (IMM) shown on the Fig. 8 for successively storing items of picture data generated by the character generator (CG) (input circuit pattern) based on the picture information given by RFM (col. 7, ll.30-33); circuit pattern extracting means for making a comparison between a circuit element of the circuit pattern being input and a corresponding circuit element contained in one of the plurality of previously stored circuit patterns stored in the unavailable area, and extracting from the plurality of previously stored circuit patterns an extracted circuit pattern in which the comparison indicates an agreement between the compared circuit elements within the display controller (DPC) shown on the Fig. 8 and depicted in details on the Fig. 11, wherein the process of comparison a circuit element of the circuit pattern as input with one from the plurality of previously stored circuit patterns in the unavailable area (CG) is performed, wherein comparator (COM), controller (CNT), buffer register (BFR) and register (RG) make a conclusion if there is an agreement or non-agreement between

those two circuit elements has been achieved (col. 9, ll.20-35); display means for displaying the extracted circuit pattern on an input screen as shown on the Fig. 10 wherein an explanatory view showing as example of a display presented on the screen of a CRT included in the system of FIG. 8 and using a drive (DDV) which receives the picture information as output of the picture memory (IMM) for displaying on the CRT (col. 7, ll.33-38; ll.44-47); and copying means for copying the extracted circuit pattern into the available area in response to an input by an operator within display controller (DPC) shown in details on the Fig. 11 which is operated as copying of transferring data into the available area (IMM) ready for display (col. 9, ll.15-20).

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen B Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HR

VUTHE SIEK
PRIMARY EXAMINER